

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
a layer of insulation material formed over a semiconductor
5 substrate; and
a metal trace formed in the layer of insulation material, the metal trace having a base region and a plurality of spaced-apart fingers that extend away from the base region.
- 10 2. The semiconductor device of claim 1 wherein the metal trace has a first end electrically connected to a first circuit, and a second end electrically connected to a second circuit, the metal trace passing a gigahertz-frequency signal from the first circuit to the second circuit.
- 15 3. The semiconductor device of claim 2 wherein the metal trace lies substantially in a plane horizontal to a surface of the substrate.
4. The semiconductor device of claim 2 wherein the fingers extend away from a top surface of the base region.
- 20 5. The semiconductor device of claim 2 wherein the metal trace is connected to a contact.
6. The semiconductor device of claim 2 wherein the metal
25 trace is connected to a via.
7. The semiconductor device of claim 1 wherein the metal trace forms a number of loops.

8. The semiconductor device of claim 7 wherein the loops lie substantially in a same plane.

9. The semiconductor device of claim 7 wherein the metal
5 trace has a first end and a second end.

10. The semiconductor device of claim 9 wherein the second end is connected to a contact.

10 11. The semiconductor device of claim 9 wherein the second end is connected to a via.

12. The semiconductor device of claim 11 wherein the via lies under the metal trace.

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13. The semiconductor device of claim 7 wherein the fingers extend away from a top surface of the base region.

14. A method of forming a semiconductor device, the method
20 comprising the steps of:

forming a layer of insulation material over a semiconductor substrate;

forming a layer of conductive material on the layer of insulation material;

25 etching the layer of conductive material to form a trace, the trace having a top surface; and

etching the trace to form a number of slot openings in the top surface of the trace.

PATENT

15. The method of claim 14 wherein the trace is formed to have a number of loops.

5 16. The method of claim 15 wherein the loops lie substantially in a same plane.

17. The method of claim 14 wherein the trace is connected to a contact.

10 18. The method of claim 14 wherein the trace is connected to a via.